

Optimized Roba Multiplier : Archiving Ultra-Fast and Power -Efficient DSP With Revolutionary Rounding – Based Approximation

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ABSTRACT: In this paper, we propose an approximate multiplier called the RoBA (Rounding-Based Approximate) multiplier, which is designed for high-speed and energy-efficient digital signal processing. The method rounds operands to the nearest exponent of two, simplifying the multiplication process while maintaining accuracy within acceptable limits. We present three hardware implementations for both signed and unsigned operations. The performance of the proposed multiplier is evaluated by comparing it with existing accurate and approximate multipliers using different design parameters. Additionally, we demonstrate its effectiveness in image processing applications such as image sharpening and smoothing, where minor computational errors do not significantly impact visual quality. The results indicate that the RoBA multiplier achieves a balance between speed, energy efficiency, and computational accuracy, making it suitable for error-resilient applications.

KEYWORDS: Approximate computing, energy-efficient multiplier, high-speed processing, digital signal processing, error analysis, RoBA multiplier.

I. INTRODUCTION

The implementation of specific circuits with LSI chips can be done by means of ICs that can be programmed to provide the required logic. The design flow for digital circuits involves several key stages to ensure successful implementation. It begins with Design Specification, where project requirements and circuit functionality are defined using tools like Wave Former, Test Bencher, or Word for waveform drawings. Next is RTL Description, where the design is coded using CAD tools with Gate Level, Data Flow, or Behavioral Modeling and verified through simulation tools like Xilinx, Verilog-XL, and ModelSim. If errors arise, the RTL description is corrected. MSI components are standard circuits, and their use results in a significant reduction in the total cost as compared to the cost of using SSI circuits.

II. LITRATURE SURVEY

Physical mechanisms responsible for non destructive single-event effects in digital microelectronics are reviewed, [1] Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing, paper proposes an approximate multiplier that enhances speed and energy efficiency by rounding operands to the nearest exponent of two. The approach is applicable to both signed and unsigned multiplications, [2] Design and Implementation of RoBA Multiplier on MAC Unit, presents a 64-bit RoBA Multiplier integrated with a MAC unit, reduce power consumption, and minimize area. The method involves rounding input values to the nearest exponent of two, resulting in high accuracy and efficiency suitable for VLSI applications. [3] Computer Multiplication and Division Using Binary Logarithms, method for performing multiplication and division using binary logarithms, reducing the complexity of these operations in computing systems. [4] Low-Power High-Speed Multiplier for Error-Tolerant Application, discusses a low-power, high-speed multiplier design suitable for applications where some computational errors are tolerable, thereby achieving significant power savings.

III. METHODOLOGY

The methodology for designing the **Optimized RoBA Multiplier : Achieving Ultra Fast and Power Efficient DSP With Revolutionary Rounding Based Approximation** focuses on achieving high performance, low power consumption, and efficient in-memory computation. The implementation is carried out through the following structured phases:

1. ENHANCED ROBA MULTIPLIER WITH INTEGRATED FIR FILTER: Rounded Based Approximate Multiplier, Which Is Used To Determine The Approximate Rounded Values. To Implement The ROBA With FIR Filter. This Means Both Signed And Unsigned Operations In Single ROBA Multiplier. That Increases The Accuracy Of The Multiplications Technique In FPGA Processor.

2. SIGN DETECTOR: The sign detector is a crucial component that identifies the sign of the input values. It operates by extracting the Most Significant Bit (MSB) of the input data. The MSB holds significant importance in binary number systems, as it determines the sign of the value.

3. ROUNDING: The rounding block is designed to simplify multiplication by rounding input values to the nearest exponent of two. This method reduces computational complexity and hardware requirements. This block also includes three barrel shifters, which are crucial for efficiently shifting input bits. The products $A_r \times B$, $B_r \times A$, and $A_r \times B_r$ are determined using these shifters by shifting the respective input bits toward the left.

4. SOFTWARE DEVELOPMENT: The software development process using Xilinx ISE starts with creating a new project that targets the FPGA device on the Spartan-3 Startup Kit demo board. To initiate this process, open the Xilinx ISE 8.1i Project Navigator and create a new project. Navigate to File > New Project, and the New Project Wizard will appear.

5. MULTIPLIER ACCUMULATOR COMPONENT (MAC): The Multiplier accumulator is a crucial component in Digital Signal Processing (DSP) system. It performs in high speed multiplication and accumulation operations, which are essential in various DSP algorithm like filtering, convolution, and fouriers analysis.

6. WALLACE TREE MULTIPLIER: The Wallace tree multiplier is a powerful and efficient architecture designed to enhance the speed and reduce the complexity of multiplication operations. This method significantly reduces the number of partial products when compared to traditional multipliers, resulting in faster computation and improved performance.

7. Design Simulation: To verify the functionality of the counter design, create a test bench waveform with the required input stimulus. Select the counter HDL file in the Sources window and create a new test bench source by choosing Project → New Source. In the New Source Wizard, select Test Bench WaveForm as the source type, name the file counter_tbw, and click Next.

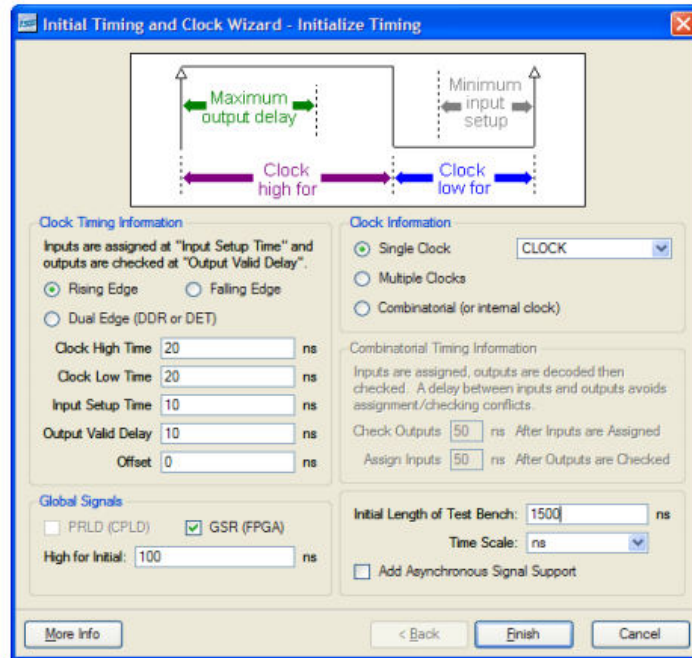


Figure: Initial Timing and Clock-Wizard

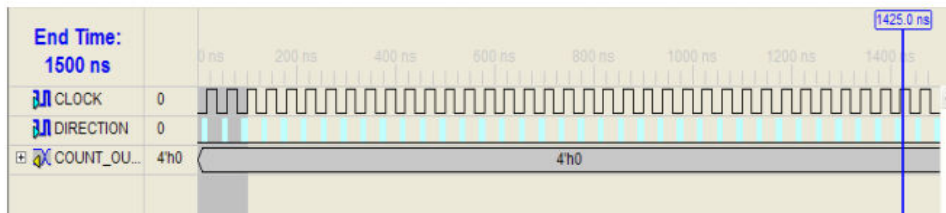


Figure: Simulation Waveform for Counter Operation

IV. EXPERIMENTAL RESULTS

The implementation of the **Optimized RoBA Multiplier : Achieving Ultra Fast and Power Efficient DSP With Revolutionary Rounding Based Approximation** demonstrates significant improvements in performance, energy efficiency, and computational speed compared to conventional architectures. The proposed system was an approximate multiplier that is high speed yet energy efficient. The approach is to round the operands to the nearest exponent of two. This way the computational intensive part of the multiplication is omitted improving speed and energy consumption at price of small error. The proposed approach is applicable to both the signed and unsigned multiplications. We propose three hardware implementations of the approximate multiplier that includes one for the unsigned and two for the signed operations. The efficiency of the proposed multiplier is evaluated by comparing its performance with those of some approximate and accurate multipliers using different design parameters. In addition, the efficacy of the proposed approximate multiplier is studied in two image processing applications, i.e., image sharpening and smoothing.

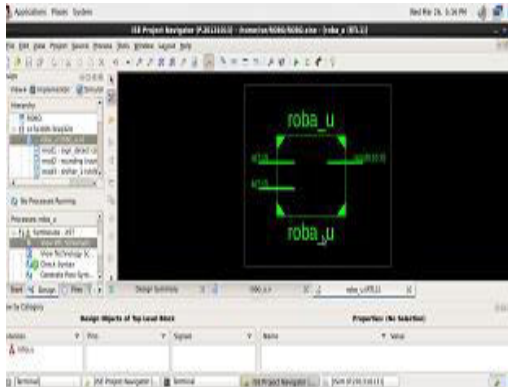


Figure: RoBA RTL I/P

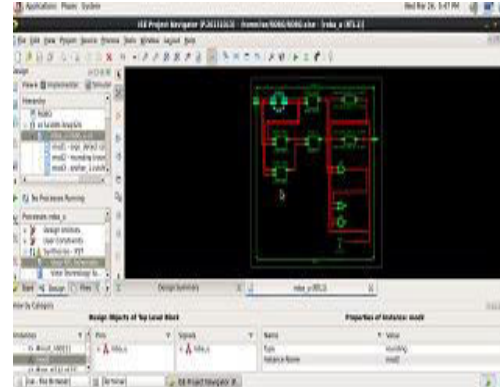


Figure: RoBA RTL Schematic

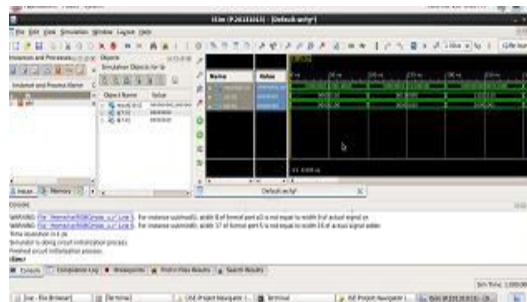


Figure: RoBA Output waveform

- Reduced latency**, due to in-memory computation and elimination of unnecessary data transfer
- Higher throughput**, enabled by parallel full-array operations
- Lower power consumption**, due to self-recycling and optimized SRAM design
- Improved energy efficiency**, making it suitable for low-power applications.

V. CONCLUSION

In this work, a **Optimized RoBA Multiplier : Achieving Ultra Fast and Power Efficient DSP With Revolutionary Rounding Based Approximation** has been successfully designed and analyzed to 64-bit ROBA (Rounding-Based Approximate) Multiplier integrated with a MAC (Multiply-Accumulate) unit. The proposed design demonstrates significant improvements in speed, area efficiency, and power consumption, making it an optimal solution for modern VLSI systems. The innovative approach of rounding the input values to the nearest exponent of two has proven to be highly effective in enhancing performance while maintaining considerable accuracy. The 64-bit ROBA multiplier with a MAC unit stands as a promising solution for modern VLSI design challenges. By achieving improved speed, reduced area, and lower power consumption without compromising accuracy, this approach aligns well with the current needs of the semiconductor industry.

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